Remarks:

Reconsideration of the application is requested.

Claims 1-7 remain in the application. Claims 1, 6 and 7 have been amended.

In item 1 on page 2 of the above-identified Office action, claim 1 has been objected to because of informalities. Appropriate correction has been made.

In item 2 on page 2 of the above-identified Office action, claims 6 and 7 have been objected to under 37 CFR 1.75 (c) as being of improper dependent form for failing to further limit the subject matter of a previous claim. Appropriate correction has been made to facilitate prosecution, although the previous form of the claims is quite commonly used and accepted.

In item 4 on pages 2-3 of the above-mentioned Office action, claims 1, 4 and 5 have been rejected as being unpatentable over Watt (US Pat. No. 5,579,526) in view of Offord (US Pat. No. 5,522,048) under 35 U.S.C. § 103(a).

As will be explained below, it is believed that the claims were patentable over the cited art in their original form and

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the claims have, therefore, not been amended to overcome the references.

The Examiner has argued that it would have been obvious to one of ordinary skill in the art to utilize the teaching of the output register and sequence controller taught by Offord in Fig. 2 of Watt for the advantage of robustly transferring data without glitches and minimizing metastability problems (see page 3, lines 5-8 of the Office action).

Watt relates to a data processing apparatus for executing successive data processing instructions. A processing core operates in accordance with a number of possible operating modes or states. A synchronous state machine is used to control the transition between the various operating states of such a processing core. The current operational state of the processing core is defined by a control state signal. The synchronous state machine generates an output state signal indicating a provisionally valid next operational state of the core.

Watt focuses on an asynchronous logic circuit for generating the control state signal fed into the processing core in response to the output state signal generated by the synchronous state machine circuit. The state machine generates a

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provisionally valid next operational state of the processing core, but that state is altered (if necessary) asynchronously by the asynchronous logic circuit (see column 1, lines 55 to column 2, line 33 and column 4, lines 16 to 26).

Offord is directed to an asynchronous-to-synchronous interface between two chips. This interface is used to synchronize data transfer of a target chip and a master chip, wherein the target chip has a clock that is running at a different speed or phase than the clock of the master chip (see column 1, lines 9 to 23). Therefore, Offord is directed to a completely different technical background and object as compared to Watt. As mentioned in column 3, lines 53 to 54 of Watt, Fig. 2 (which is referred to by the examiner) is a schematic diagram of a central processing unit, wherein such CPU is certainly placed on a single chip. In contrast to this, Offord is directed to an apparatus for providing an asynchronous-to-synchronous interface between a master chip and a target chip (see column 3, lines 29 to 32 of Offord). Hence, Watt and Offord have nothing in common with regard to technical background and object. Therefore, one skilled in the art is certainly not taught to combine these two references when solving the problem according to the invention of the instant application.

Moreover, even when combining these two references, Offord does not teach a sequence controller connected to an asynchronous

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circuit, which is cnstructed to generate a first control clock signal and a second control clock signal in dependence on a duration required for the data to be processed in such asynchronous circuit. The sequence controller according to the invention of the instant application is not a "simple" sequence controller, but is constructed to adapt the data exchange between the asynchronous circuit and the synchronous circuit to the processing speed of the asynchronous circuit. In contrast, Offord provides an interface circuit which synchronizes two synchronous chips having clock signals which are running at different speeds or phases (see, for example, column 3, lines 29 to 32 in connection with column 1, lines 16 to 23).

It is accordingly believed to be clear that none of the references, whether taken alone or in any combination, either show or suggest the features of claim 1. Claim 1 is, therefore, believed to be patentable over the art and since claims 4 and 5 are dependent on claim 1, they are believed to be patentable as well.

Applicants acknowledge the Examiner's statement in item 5 on pages 3-4 of the above-mentioned Office action that claims 2 and 3 would be allowable if written in independent form including all of the limitations of the base claim and any intervening claims.

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Since claim 1 is believed to be patentable as discussed above and claims 2 and 3 are ultimately dependent on claim 1, they are believed to be patentable in dependent form. A rewrite is therefore believed to be unnecessary at this time.

In view of the foregoing, reconsideration and allowance of claims 1-7 are solicited.

In the event the Examiner should still find any of the claims to be unpatentable, counsel would appreciate a telephone call so that, if possible, patentable language can be worked out.

Please charge any fees which might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.

Respectfully submitted,

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December 16, 2002

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Applic. No.: 10/033,123

Marked-Up Version of the Amended Claims:

Claim 1(amended). An integrated circuit, comprising:

a synchronous circuit;

an asynchronous circuit;

an input register circuit connected to said synchronous circuit and said asynchronous circuit, said input register circuit having a terminal receiving a first control clock signal for controlling data transfer;

an output register circuit connected to said synchronous circuit and said asynchronous circuit, said output register circuit having a terminal receiving a second control clock signal for controlling data transfer; and

a sequence controller;

[said synchronous circuit storing data in] said input register circuit [so that the data can be processed] storing data of said synchronous circuit for processing in said asynchronous circuit;

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[said asynchronous circuit storing the processed data in] said output register circuit [so that the processed data can be further processed] storing data of said asynchronous circuit for further processing in said synchronous circuit; and

said sequence controller connected to said asynchronous circuit for generating the first control clock signal and the second control clock signal in dependence on a duration required for the data to be processed in said asynchronous circuit.

Claim 6(amended). A method for operating [the] an integrated circuit [according to claim 1], the method which comprises:

activating [said] a first control clock signal to transfer [the] data from [said] a synchronous circuit into [said] an input register circuit;

transferring the data from [said] the input register circuit into [said] an asynchronous circuit and processing the data in [said] the asynchronous circuit to obtain [the] processed data;

with [the] a sequence controller, inactivating the first control clock signal within the duration required for the data to be processed in [said] the asynchronous circuit; and

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not earlier than [at] a completion of the duration required for the data to be processed in [said] the asynchronous circuit, using [the] a second control clock signal to trigger transfer of the processed data into [said] an output register circuit.

Claim 7 (amended). The method according to claim 6, which comprises:

providing a terminal for receiving a clock signal having an active state and an inactive state;

providing a controllable switch for switchably connecting together [said] the terminal for receiving the clock signal and [said] a terminal receiving the first control clock signal;

inactivating [said] the first control clock signal by opening [said] the controllable switch; and

using [said] the sequence controller to close [said] the controllable switch in the inactive state of the clock signal.

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